



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,245	08/29/2001	Tongbi Jiang	2421.1US (99-0408.1)	8370
24247	7590	09/09/2004	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			IM, JUNGHWA M	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-8, 10-12, 14-16, 20, 21, 23, 24, 26-28, 30-33, 35-37, 39-41 and 45-49 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada et al. (US 5,864,178), hereinafter Yamada.

Regarding claims 1-3, 6-8, 10-12, 14-16, 20, 21, 23, 24, 26-28, 31-33, 35-37, 39-41 and 45-49, Fig. 58 of Yamada shows a semiconductor assembly comprising:

a semiconductor device (or a die; 201) having an active surface having a plurality of bond pads (224);

a substrate (202; a wiring circuit board) having an upper surface having a plurality of circuits;

a plurality of bumps (203) connecting said plurality of bond pads on said active surface of said semiconductor device to said plurality of circuits on said upper surface of said substrate;

said plurality of bumps forming a gap between said semiconductor device and said substrate;

an underfill material (encapsulation resin; col. 56, lines 20-26) to fill the gap between said substrate and said semiconductor device (or between the substrate and the wetting agent layer);

Art Unit: 2811

a wetting agent layer of about a monolayer thick, said wetting agent layer wettable by a polymeric material (207, 208) provided on the active surface of said semiconductor device and on a upper surface of substrate (col. 56, lines 22-63 and col. 17, lines 53-59); and

said wetting agent including silane (col. 56, lines 29-63).

Regarding claims 5 and 30, Yamada discloses the wetting agent layer reduces surface tension of the active surface throughout the specification especially in col. 20, lines 34-65.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 9, 13, 19, 22, 29, 34, 38 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Wong et al. (US 6,180,696), hereinafter Wong.

Regarding claims 4, 9, 13, 19, 22, 29, 34, 38 and 44, Yamada shows substantially the entire claimed structure except a specified wetting material. Wong discloses ethyltrimethoxysilane as a wetting material for an underfill process applied for a flip chip packaging. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teachings of Wong for the wetting layer of Yamada in order to have to good adhesion between chips and substrates, therefore reducing a surface tension in-between as taught in a portion of col. 15, lines 18-22 of Wong's reference.

Response to Arguments

Applicant's arguments filed June 14, 2004 have been fully considered but they are not persuasive.

1. Applicant argues that "The silane coupling agent [of Yamada] is only used in the formation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit." Examiner disagrees. First, it is pointed that the instant claim recites "a wetting agent layer ... wettable by a polymeric material" and the wettable agent layer is formed of silane which is resin. With this understanding, starting in column 56, line 22, Yamada explicitly discloses that a polymer film (207, 208) is formed on the semiconductor chip and on the wiring circuit board. And this polymer film has wettability to the resin (col. 17, lines 53-58).

2. Regarding the argument on 35 U.S.C. 103 rejection based on Estes in view of Wang, it is pointed that the rejection should have been written as being unpatentable over Yamada in view of Wong. However, all the detailed further statement clearly recited Yamada. Therefore, it should be understood that the rejection is based on Yamada in view of Wang.

3. Applicant further argues that "The Wong reference does not teach or suggest the use of a silane coupling agent as part of the epoxy base polymeric composition." However, Wong discloses ethyltrimethoxysilane (silane based material) as a wetting material for an underfill process applied for a flip chip packaging (col. 15, lines 18-22).

4. In response to Applicant's argument that there is no suggestion to combine the references of Yamada and Wong, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 189 USPQ

Art Unit: 2811

607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA1971). References are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 595 (CCPA) 1969.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

Art Unit: 2811

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800